in response to receipt from the host processor of user data and a command to write said user data to said at least one mass memory storage block address, writing at least one sector of said user data into the addressed at least one of the memory array cell groups, and

in response to receipt from the host processor of a command to read user data from said at least one mass memory storage block address, reading at least one sector of said user data and associated overhead data from the addressed at least one of the memory array cell groups.

74. 16 (Amended) The method according to any one of claims 1 63-65 or 2 67-71, wherein the amount of user data stored in individual ones of the groups of array cells is substantially the same as the amount of user data contained in individual ones of [said] individual mass memory storage blocks of data transferred between the bulk storage memory and the host processor.

23 77. (Amended) The method according to claim 76, wherein said bulk storage memory is provided within a card that is removably connectable to the [computer system] host processor through an electrical connector.

18 80. (Amended) The method according to claim 16 74, wherein said bulk storage memory is provided within a single card that is removably connectable to the [computer system] host processor through an electrical connector.

Add the following new claims:

99
--161. A method of operating, with a host processor, a non-volatile memory system that includes an array of non-volatile floating gate memory cells partitioned into sectors of memory cells that are erasable together as a unit, comprising:

providing said memory array and a memory controller within a card that is removably connectable to the host processor, the controller being connectable to said host processor for controlling operation of the memory array when the card is connected to the host processor, and the memory cells within said memory array being individually programmable into one of more than two distinct threshold level ranges corresponding to more than one bit of data per cell,

causing the controller, in response to receipt from the host processor of an address in a format designating at least one mass memory storage sector, to designate an address of at least one non-volatile memory sector that corresponds with said at least one mass memory storage block,

either writing user data to, or reading user data from, said at least one non-volatile memory sector,

either writing to, or reading from, said at least one non-volatile memory sector, overhead data related either to said at least one non-volatile memory sector or to user data stored in said at least one non-volatile memory sector, and

wherein the writing of user and overhead data includes programming the individual memory cells of the array into said one of more than two distinct threshold level ranges.

100 ~~162~~. The method of claim 99 ~~161~~, wherein the overhead data written into said at least one non-volatile memory sector is generated within the memory controller.

101 ~~163~~. The method of claim 99 ~~161~~, wherein the user data written into the individual sectors is substantially 512 bytes.

102 ~~164~~. The method of claim 99 ~~161~~, wherein the overhead data stored in said overhead portion of the individual sectors includes addresses of the individual sectors.

103 ~~165~~. The method of claim ~~164~~, wherein the overhead data stored in said overhead portion of the individual sectors additionally includes, in those sectors that are defective, addresses of sectors being substituted therefor.

104 ~~166~~. The method of claim 99 ~~161~~, additionally comprising causing the controller to identify and store addresses of any defective non-volatile memory sectors within the array, and, wherein designating an address of said at least one memory sector includes, in response to designating an address of a defective sector, substituting an address of another sector instead.

105 ~~167~~. The method of claim 99 ~~161~~, wherein the address of said at least one mass memory storage block includes an address of at least one magnetic disk sector.

106 ~~168~~. The method of claim 99 ~~161~~, further comprising erasing data from a selected at least one of the individual sectors of memory cells by simultaneously applying an erase voltage to all of the memory cells within said selected at least one sector, thereby to simultaneously erase any user data and associated overhead data contained in said at least one sector.

107 ~~169~~. The method of claim ~~168~~, wherein the memory array cells individually include erase gates, and the erase voltage is simultaneously applied to the erase gates of said selected at least one sector of memory cells.--